< W3150A+ / W5100 Application Note for SPI >

Introduction

This application note describes how to set up the SPI in W3150A+ or W5100. Both the W3150A+ and W5100 have same architecture.

W5100 is operated as an SPI slave device. So, you should connect the W5100 to the SPI master device (normally MCU). For SPI operation, the SEN pin should be asserted high in the W5100.

Serial Peripheral Interface mode uses only four pins for data communication. The four pins are: SCLK, /SCS, MOSI, MISO.

- SCLK – Serial Clock (output from master)
- /SCS – Slave Chip Select (output from master, active low)
- MOSI – Master Output, Slave Input (output from master)
- MISO – Master Input, Slave Output (output from slave)

Common alternative names for these pins include:

- SCK, CLK – Serial Clock
- SS, nCS, CS, nSS, STE – Slave Chip Select, Slave Transmit Enable
- SDI, DI, SI – Serial Data In
- SDO, DO, SO – Serial Data Out

The SDI/SDO (DI/DO, SI/SO) convention requires that the SDO on the master be connected to the SDI on the slave, and vice-versa. Because the W5100 operates only as SPI slave, the MOSI may be recognized as SI, and the MISO may be recognized as SO.

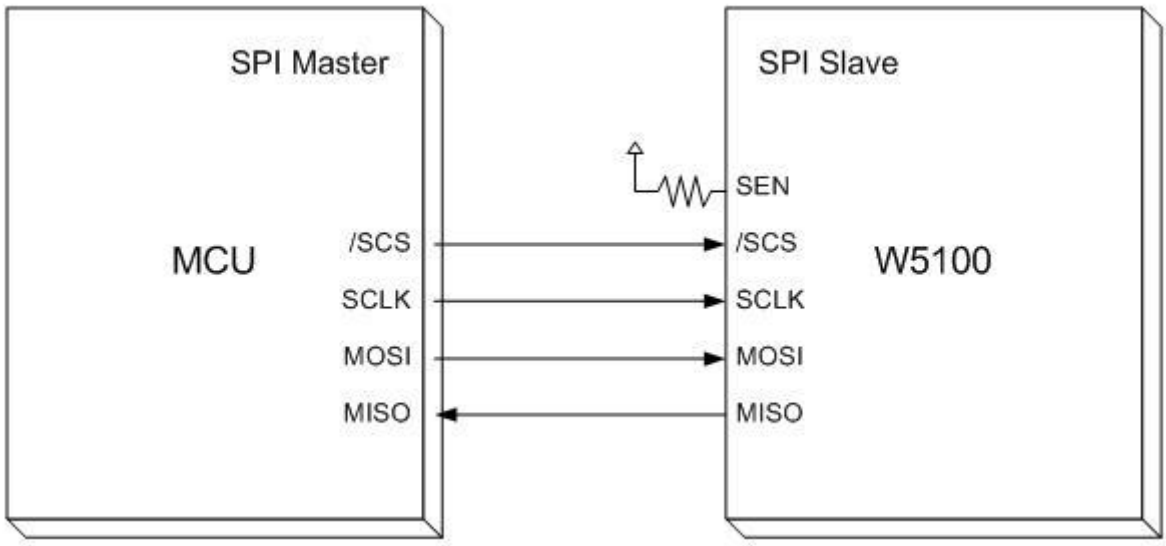

Figure 1. Basic SPI Implementation

Device Operations

The W5100 is controlled by a set of instructions that are sent from a host controller, commonly referred to as the SPI Master. The SPI Master communicates with W5100 via the SPI bus which is composed of four signal lines: Slave Chip Select (/SCS), Serial Clock (SCLK), MOSI (Master Out Slave In), MISO (Master In Slave Out).

The SPI protocol defines four modes for its operation (Mode 0, 1, 2, 3). Each mode differs according to the SCLK polarity and phase (how the polarity and phase control the flow of data on the SPI bus). The W5100 operates as SPI Slave device and supports Mode 0 only.

With SPI Mode 0, data is always latched in on the rising edge of SCLK and always output on the falling edge of SCLK.

The SPI bus can operate with a single master and with one or more slave devices. If there are more than one slave devices in your design, you should carefully specify W5100 SPI signals. For more information about this, refer to 'Multiple SPI Slave Usage' below.

Single SPI Slave Usage

When your design has a single SPI device using only the W5100, you can refer to Figure 2.

Table 1 contains the major pins that should be checked.

PIN NAME	RECOMMENDED STATUS	DESCRIPTION
SEN	PULL UP	For SPI operation, SEN has to asserted as high. Pull up resister is used to 4.7K ohm.
ADDRESS 0:14	PULL DOWN	We recommend ADDRESS pins are pulled down.
DATA 0:7	PULL DOWN	We recommend DATA pins are pulled down.
/CS, /WR, /RD	PULL UP	These pins are for BUS communication. In SPI mode, these are not used.
/RESET	Signal asserted by MCU or hardware reset circuit	You should implement reset circuit or assert from MCU GPIO pin. Because the W5100 does not support Power-on-Reset, this pin should assert low for at least 2us when power is applied to the W5100.
/INT	optional	W5100 generates an interrupt signal. If you want to use this signal for MCU, you can connect to the interrupt pin of the MCU. If you don't use the interrupt signal, this pin can be floated or pulled up.

Table 1. Recommended Status of Major Pins

Because the SPI uses four pins for communication, unused pins should be pulled over. Some pins are internally pulled down, such as ADDRESS pins. However, we recommend that unused pins are pulled down/up for preventing of EMI effects.

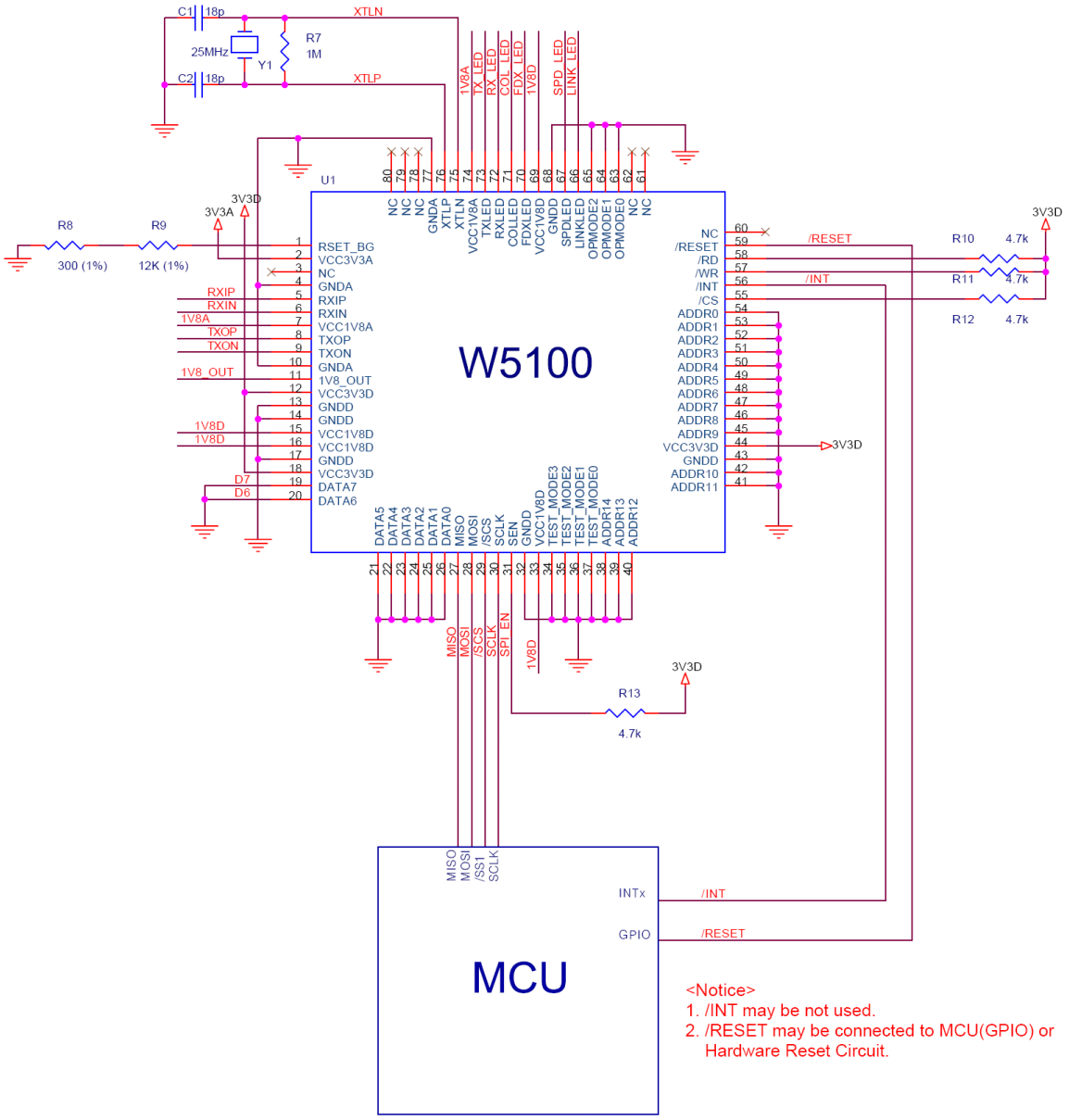

Figure 2. SPI Reference Schematic for Single SPI Slave Device.

Multiple SPI Slave Usage

Basically, multiple SPI slave usage is the same as single SPI slave usage. One difference between other SPI slave devices compared to the W5100 is that the MISO output is continuously driven in the W5100 whether the /SCS is asserted as high or as low. As well, when the 5100 /SCS is asserted as high when using multiple slaves, other SPI devices cannot be read or written by the SPI master on the SPI BUS simultaneously. These problems will continue unless the recommendations listed below are followed.

Recommendations:

- When accessing another device on the SPI BUS rather than the W5100, assert the SEN pin in the W5100 as low first, then access the other devices.
- When accessing the W5100, the SEN pin should be high.

Figure 3 is a reference schematic for multiple SPI slave devices. The W5100's SEN signal is input from the /SCS through the inverter. If you don't want to use the inverter, you can control each signal through the I/O port of the MCU.

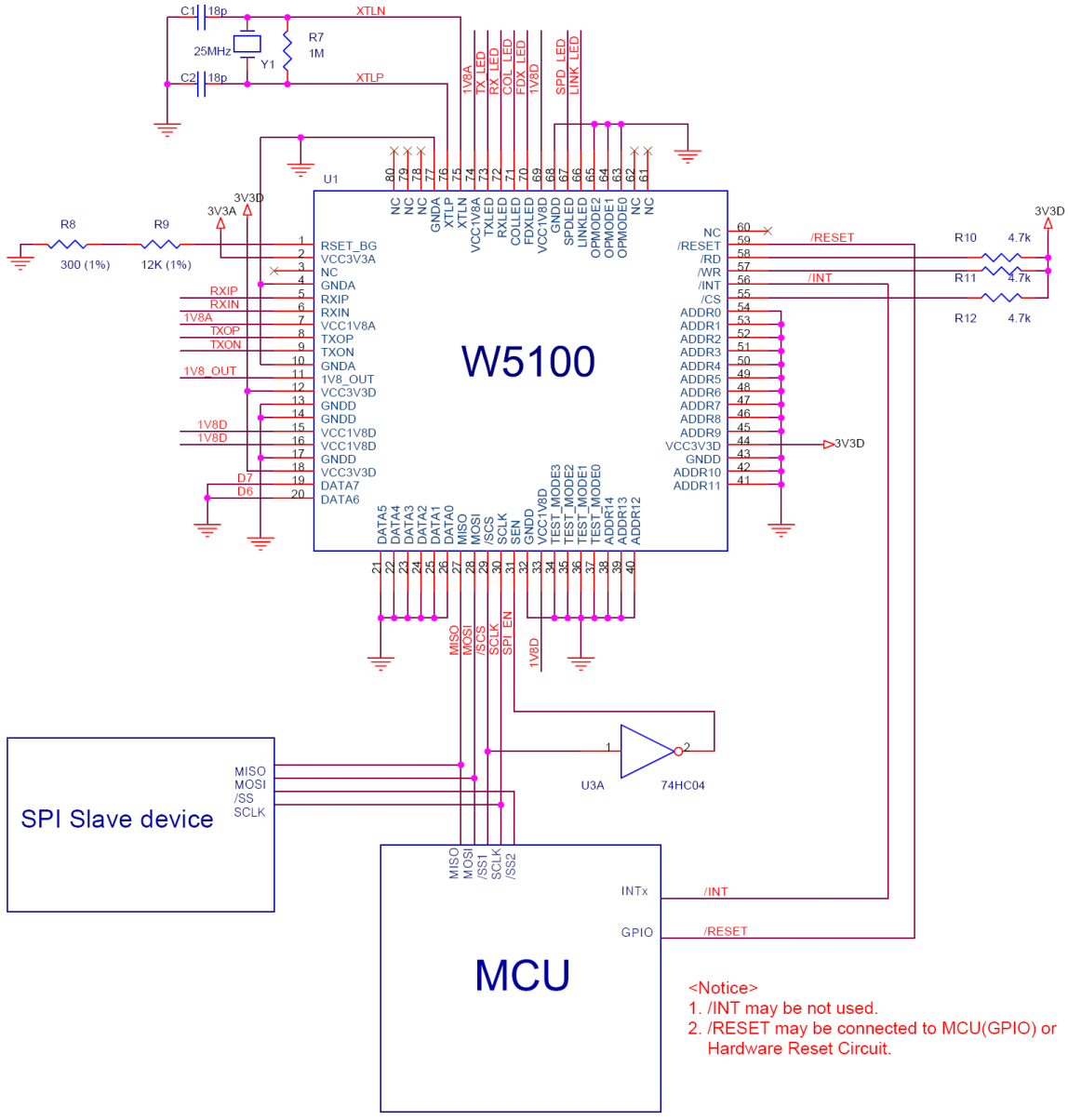

Figure 3. SPI Reference Schematic for Multiple SPI Slave Devices.

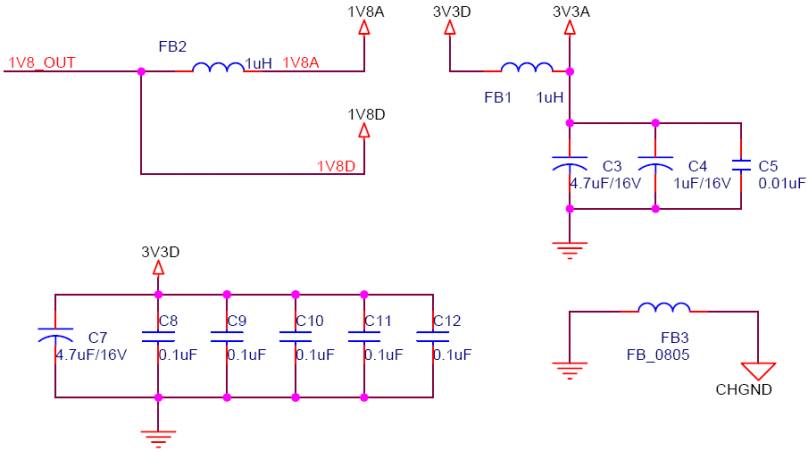

Figure 4. Reference Schematic for POWER Parts

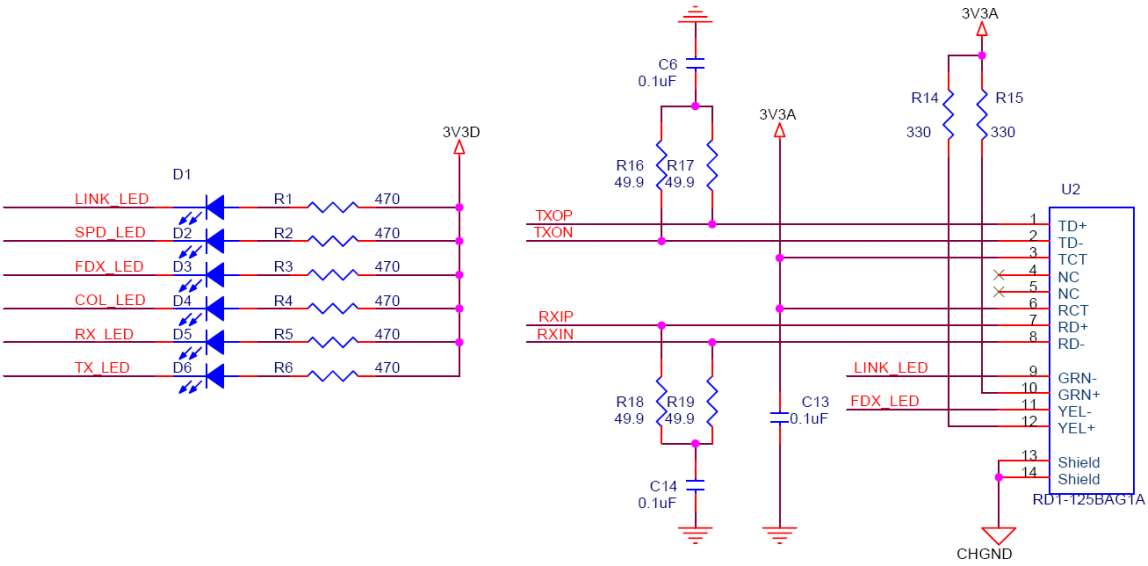

Figure 5. Reference Schematic for LED & Mag-Jack

Commands

According to SPI protocol, there are only two data lines used between SPI devices. So, it is necessary to define the OP-Code. W5100 uses two types of OP-Codes: Read OP-Code and Write OP-Code. If neither of these OP-Codes are used, the W5100 will be ignored and no operation will be started.

In SPI Mode, W5100 operates in “unit of 32-bit stream”.

The unit of 32-bit stream is composed of 1 byte OP-Code Field, 2 bytes Address Field, and 1 byte data Field.

OP-Code, Address and data bytes are transferred by the most significant bit(MSB) first and least significant bit(LSB) last.

W5100 SPI data format is below:

Command	OP-Code Field		Address Field	Data Field
Write operation	0xF0	1111 0000	2 bytes	1 byte
Read operation	0x0F	0000 1111	2 bytes	1 byte

Table 2. W5100 SPI Data Format

Process of using general SPI Master device (According to SPI protocol)

1. Configure Input/Output direction on SPI Master device pins.
    * /SCS (Slave Chip Select) : Output pin
    * SCLK (Serial Clock) : Output pin
    * MOSI (Master Out Slave In) : Output pin
    * MISO (Master In Slave Out) : Input pin
2. Configure /SCS as ‘High’
3. Configure the registers on SPI Master device.
    * SPI Enable bit on SPCR register (SPI Control Register)
    * Master/Slave select bit on SPCR register
    * SPI Mode bit on SPCR register
    * SPI data rate bit on SPCR register and SPSR register (SPI State Register)
4. Write desired value for transmission on SPDR register (SPI Data Register).
5. Configure /SCS as ‘Low’ (data transfer start)
6. Wait for reception completion
7. If all data transmission ends, configure /SCS as ‘High’

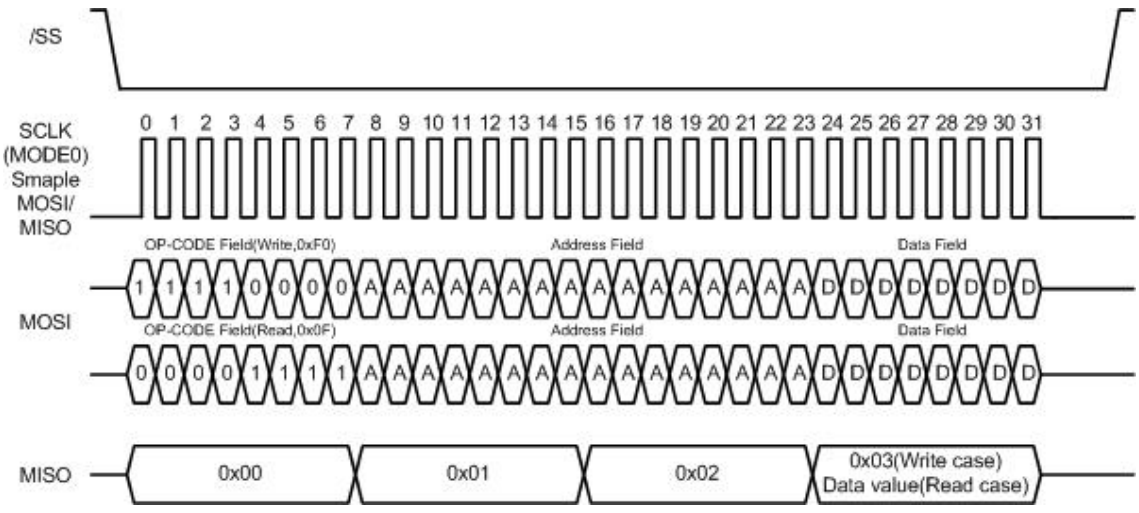

Figure 6. W5100 SPI Timing Diagram